I. Amendments to the Claims

1. (Cancelled)

2. (Currently Amended) The video input protection circuit according to Claim [[1]] 5, wherein the first transistor is configured to limit voltage applied to the termination resistor.

3. (Currently Amended) The video input protection circuit according to Claim [[1]] 5, wherein the first transistor includes an N channel MOSFET transistor.

4. (Currently Amended) The video input protection circuit according to Claim [[1]] 5, wherein a drain of the first transistor is connected to the video input terminal and a source of the first transistor is in communication with the termination resistor.

5. (Currently Amended) ~~The video input protection circuit according to Claim 1, further comprising~~ A video input protection circuit connected to a video circuit, the video input protection circuit comprising:

a video input terminal for receiving a video signal;

a first transistor in electrical series with the video input terminal;

a termination resistor in electrical connection with the first transistor, wherein the first transistor is connected between the video input terminal and the termination resistor; and

a second transistor in electrical communication with the first transistor.

6. (Original) The video input protection circuit according to Claim 5, wherein a gate of the first transistor is in communication with the second transistor and a power source.

7. (Original) The video input protection circuit according to Claim 6, further comprising a voltage divider circuit.

8. (Original) The video input protection circuit according to Claim 7, wherein the voltage divider circuit is connected to the video circuit.

9. (Original) The video input protection circuit according to Claim 7, wherein the voltage divider circuit is in communication with the second transistor.

10. (Original) The video input protection circuit according to Claim 9, wherein the voltage divider circuit includes a first and second resistor, the first resistor being connected to the termination resistor on a first end and a base of

the second transistor on a second end, the second resistor being connected to a base of the second transistor on a first end and an electrical ground on a second end.

11. (Currently Amended) The video input circuit according to Claim [[1]] 5, further comprising a first zener diode connected between the video input terminal and an electrical ground.

12. (Original) The video input protection circuit according to Claim 11, further comprising a second zener diode in electrical series connection with the first the zener diode between the video input terminal and the electrical ground.

13. (Original) The video input protection circuit according to Claim 12, wherein an anode of the first zener diode is in communication with the video input terminal and the cathode of the first zener diode is in communication with the electrical ground, an anode of the second zener diode is in communication with the electrical ground and the cathode of the second zener diode is in communication with the video input terminal.

14. (Cancelled)

15. (Currently Amended) The video input protection circuit according to Claim [[14]] 17, wherein a drain of the N channel MOSFET transistor is connected to the video input terminal and a source of the N channel MOSFET transistor is in communication with the termination resistor.

16. (Currently Amended) The video input protection circuit according to Claim [[14]] 17, wherein the N channel MOSFET transistor is configured to limit voltage applied to the termination resistor.

17. (Currently Amended) ~~The video input protection circuit according to Claim 14, further comprising~~ A video input protection circuit connected to a video circuit, the video input protection circuit comprising:

a video input terminal for receiving a video signal;

a N channel MOSFET transistor in electrical series with the video input terminal;

a termination resistor in electrical connection with the N channel MOSFET, wherein the N channel MOSFET is connected between the video input terminal and the termination resistor; and

a second transistor in electrical communication with the N channel MOSFET.

18. (Original) The video input protection circuit according to Claim 17, wherein a gate of the N channel MOSFET transistor is in communication with the second transistor and a power source.

19. (Original) The video input protection circuit according to Claim 17, further comprising a voltage divider circuit.

20. (Original) The video input protection circuit according to Claim 19, wherein the voltage divider is connected to the video circuit.

21. (Original) The video input protection circuit according to Claim 19, wherein the voltage divider circuit is in communication with the second transistor.

22. (Original) The video input protection circuit according to Claim 21, wherein the voltage divider circuit includes a first and second resistor, the first resistor being connected to the termination resistor on a first end and a base of the second transistor on a second end, the second resistor being connected to the base of the second transistor on a first end and an electrical ground on a second end.

23. (Currently Amended) The video input circuit according to Claim [[14]] 17, further comprising a first zener diode connected between the video input terminal and an electrical ground.

24. (Original) The video input protection circuit according to Claim 23, further comprising a second zener diode in electrical series connection with the first the zener diode between the video input terminal and the electrical ground.

25. (Original) The video input protection circuit according to Claim 24, wherein an anode of the first zener diode is in communication with the video input terminal and the cathode of the first zener diode is in communication with the electrical ground, an anode of the second zener diode is in communication with the electrical ground and the cathode of the second zener diode is in communication with the video input terminal.

26. (New) The video input protection circuit according to Claim 5, wherein the second transistor is configured to clamp the voltage of the first transistor.

27. (New) The video input protection circuit according to Claim 17, wherein the second transistor is configured to clamp the voltage of the N channel MOSFET.